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context switching &lt;near&gt; thread interleaving

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A Agarwal, BH Lim, D Kranz, J Kubiatowicz - portal.acm.org

... not support cycle-by-cycle **interleaving of threads** ... ecutes instructions from a given **thread** until it ... a sim- ple processor design with **context switch** overheads of ...[Cited by 589](#) - [Related articles](#) - [Web Search](#) - [All 14 versions](#)**[Interleaving: a multithreading technique targeting multiprocessors and workstations](#)**

J Laudon, A Gupta, M Horowitz - ACM SIGPLAN Notices, 1994 - portal.acm.org

... the need for large numbers of active contexts and the poor single-**thread** per- formance, are not intrinsic limitations of cycle-by-cycle **context switching**. ...[Cited by 100](#) - [Related articles](#) - [Web Search](#) - [BL Direct](#) - [All 6 versions](#)**[An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads - \\*kit.ac.jp \[PDF\]](#)**

H Hirata, K Kimura, S Nagamine, Y Mochizuki, A ... - portal.acm.org

... ters an absence of data, the processor rapidly **switches** ... fetches at most B instruc- tions for one **thread** every C ... in an **interleaved** fashion for multiple **threads**. ...[Cited by 174](#) - [Related articles](#) - [Web Search](#) - [BL Direct](#) - [All 6 versions](#)**[Multithreaded processor architectures](#)**

GT Byrd, MA Holliday - Spectrum, IEEE, 1995 - ieeeexplore.ieee.org

... instructions from the same **thread** and **switching** ... the hardware; the cost of **switching** be- tween ... of cycles typically executed between **context switches**, called the ...[Cited by 88](#) - [Related articles](#) - [Web Search](#) - [BL Direct](#) - [All 2 versions](#)**[Hybrid technology multithreaded architecture](#)**

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... of realistically achieving near-petaflops per ... overheads for process **switching**, synchronization and ... **Interleaved thread** execution requires a fundamental change ...[Cited by 38](#) - [Related articles](#) - [Web Search](#) - [All 7 versions](#)**[Replay for concurrent non-deterministic shared-memory applications](#)**

M Russinovich, B Cogswell - Proceedings of the ACM SIGPLAN 1996 conference on ..., 1996 - portal.acm.org

... by different pro- cesses or **threads** may be ... application the coarse-grained **interleaving** characteristics can be ... schedule, ensuring that **context switches** occur at ...[Cited by 49](#) - [Related articles](#) - [Web Search](#) - [Library Search](#) - [BL Direct](#) - [All 3 versions](#)**[Dataflow architectures and multithreading](#)**

B Lee, AR Hurson - Computer, 1994 - ieeeexplore.ieee.org

... **Interleaving** can be done in many ways, that is, on every cycle, on remote reads, and so ... **Context switching** can occur on every cycle or when a **thread** dies due ...[Cited by 55](#) - [Related articles](#) - [Web Search](#) - [BL Direct](#) - [All 7 versions](#)**[MSparc: A Multithreaded Sparc](#)**

A Mikschl, W Datum - LECTURE NOTES IN COMPUTER SCIENCE, 1996 - Springer

... latency operations by **switching** from one **context** to another. one design issue of multithreaded architectures is whether **interleaving of thread** execution is ...[Cited by 27](#) - [Related articles](#) - [Web Search](#) - [BL Direct](#) - [All 6 versions](#)**[Multi-threaded microprocessor architecture utilizing static interleaving](#)**

JC Chung, CL Wu - US Patent 5,404,469, 1995 - freepatentsonline.com

... and gate counts expected in the **near** future for ... Because no **context-switch** overhead

exists among **threads** which ... **interleaving** unit selects a **thread** according to a ...

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### **Context-switching techniques for decoupled multithreaded processors**

J Kreuzinger, T Ungerer - Euromicro'99, 1999 - doi.ieeecs.org

... poor. The block **interleaving** approach executes a single **thread** until it reaches a situation that triggers a **context switch**. Usually ...

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